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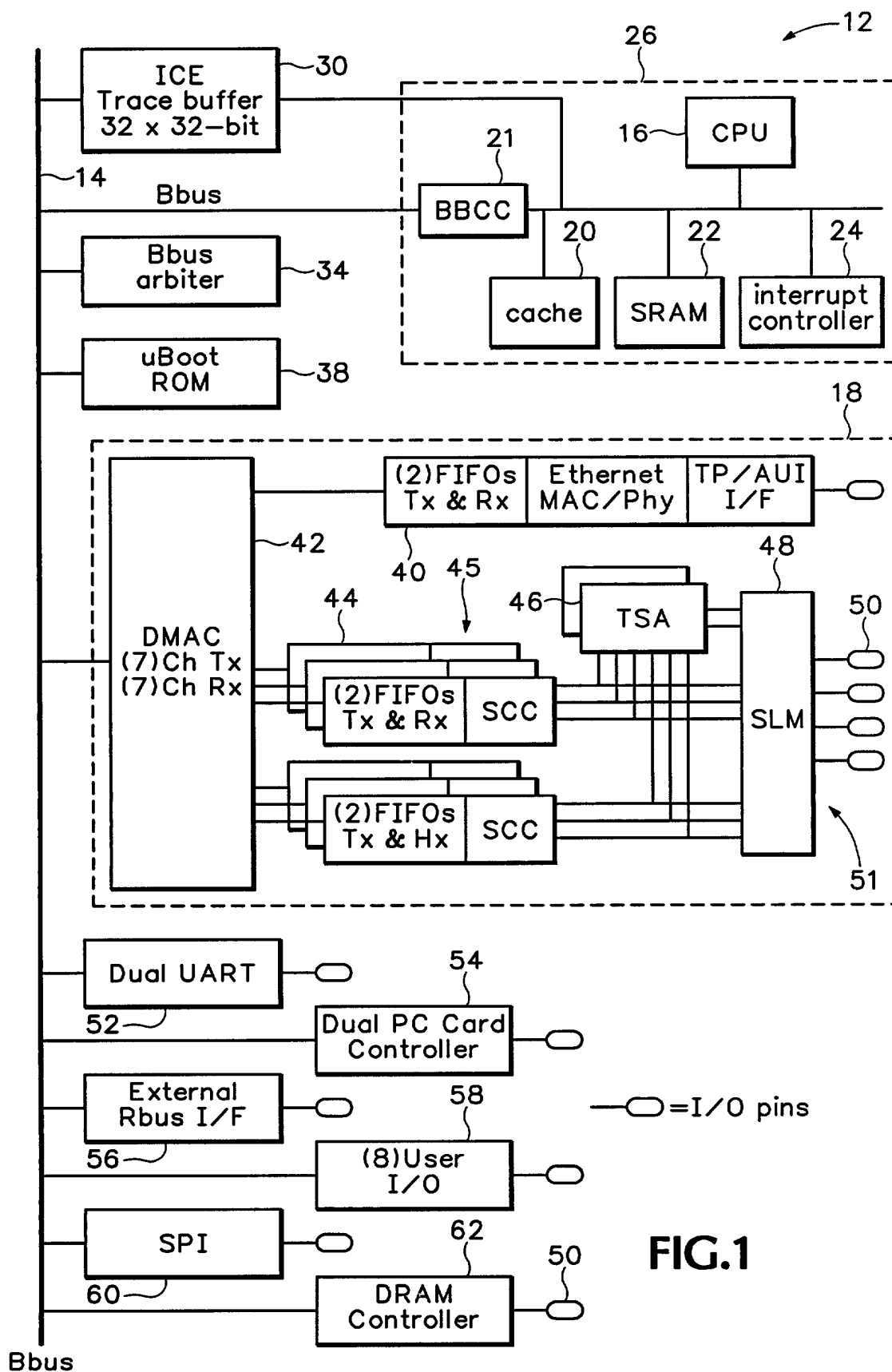


FIG.1

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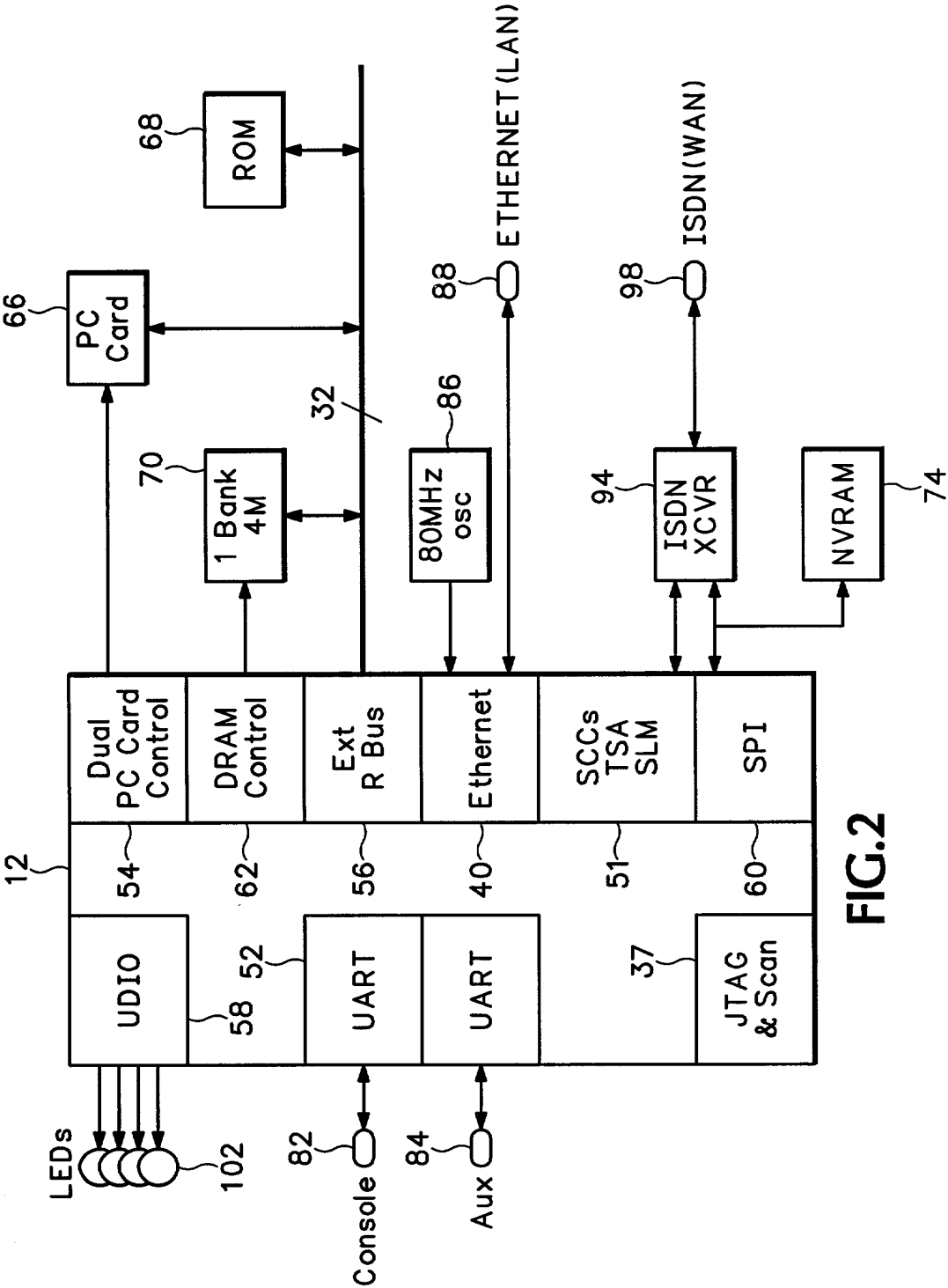


FIG.2

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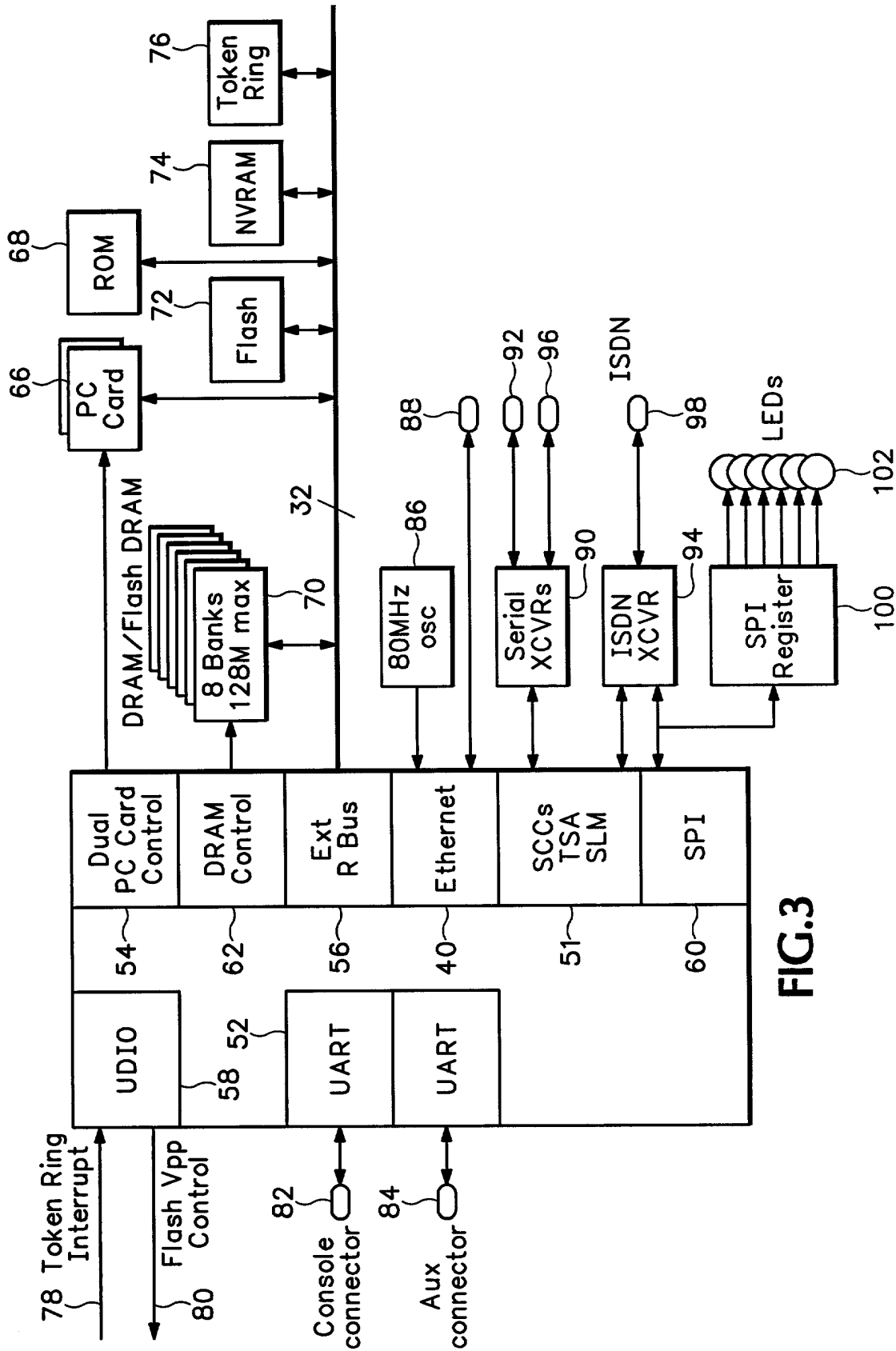
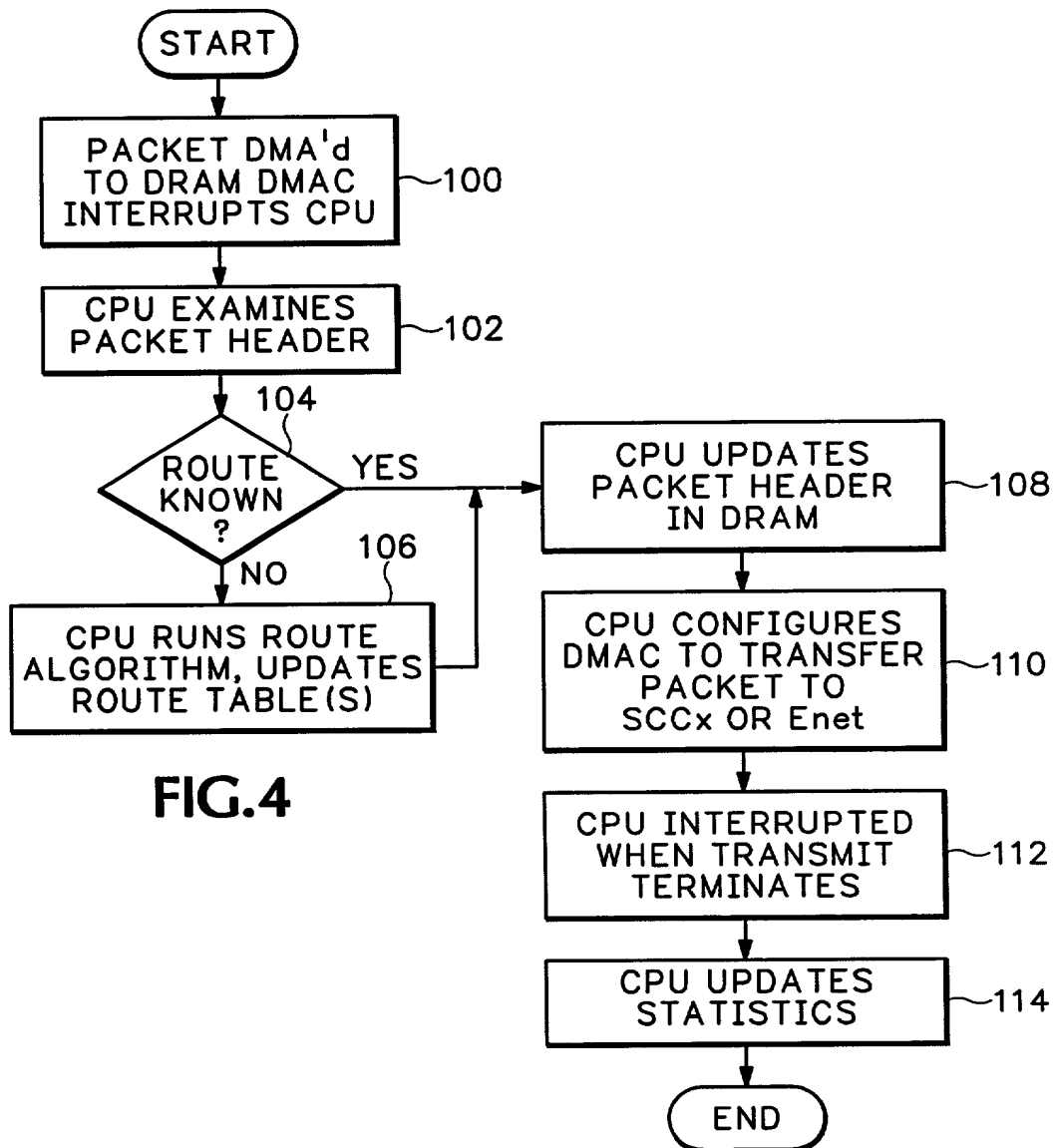


FIG.3

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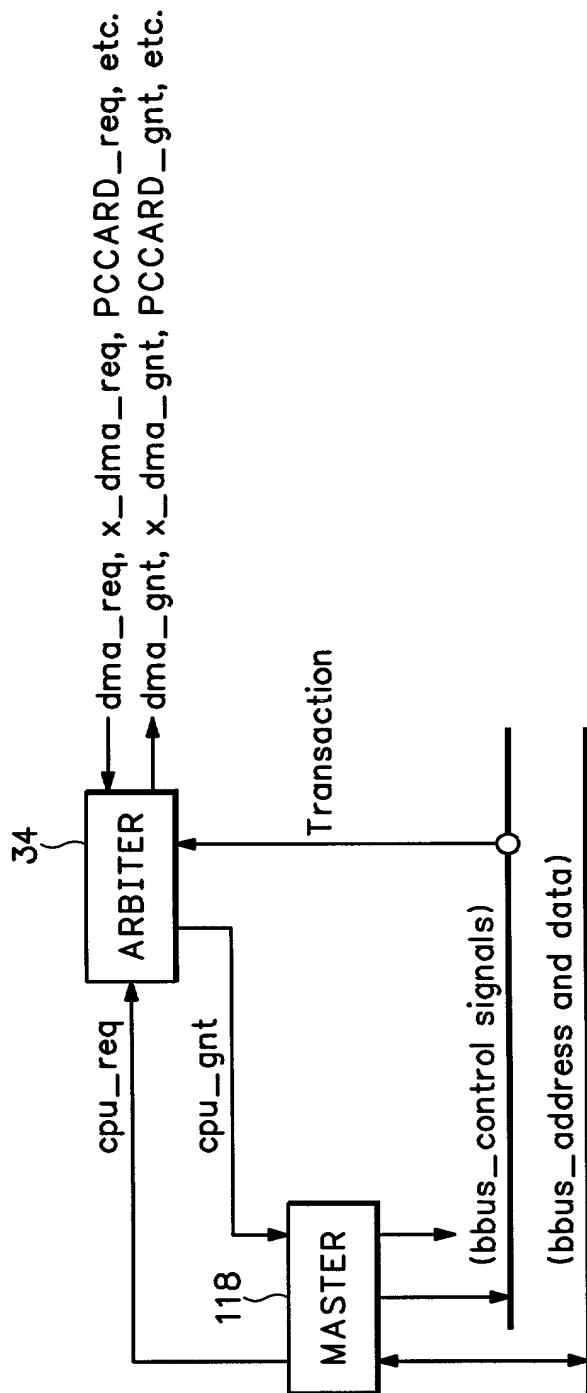


FIG.5
MODULE INTERFACE

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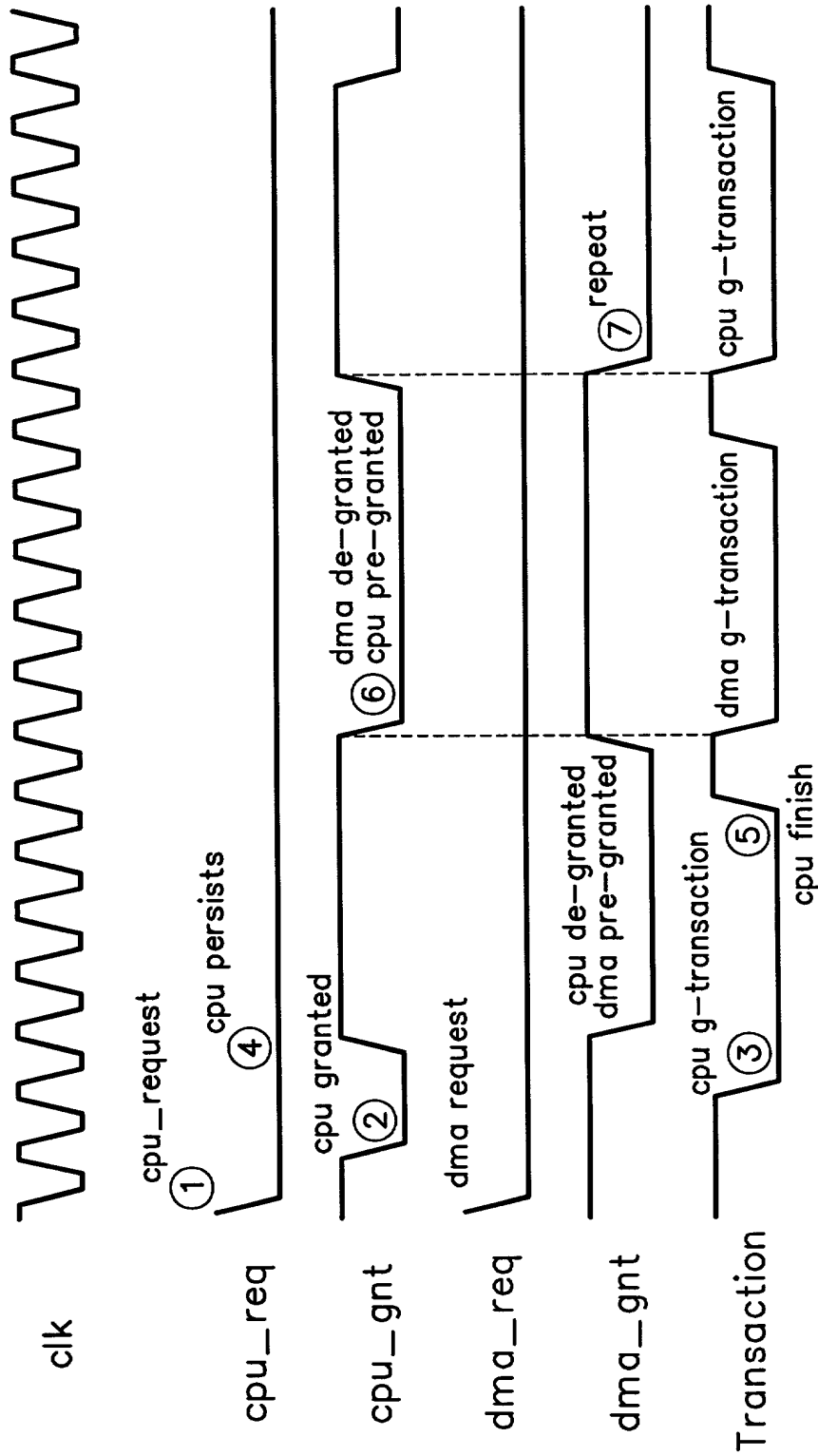


FIG.6
PIPELINED ARBITRATION
PROTOCOL EXAMPLE

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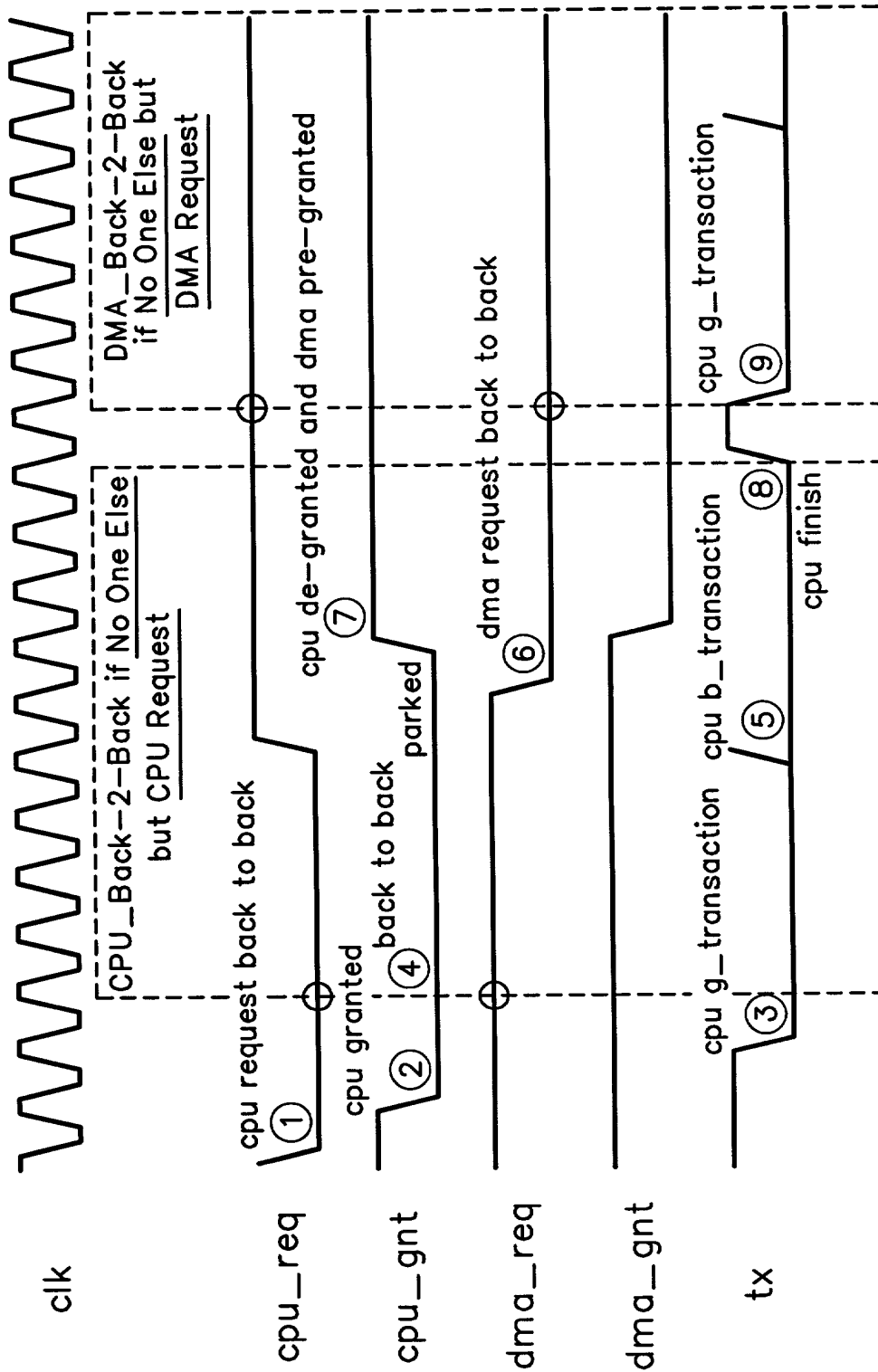


FIG.7
 ARBITRATION PROTOCOL EXAMPLE
 BACK-TO-BACK TRANSACTION

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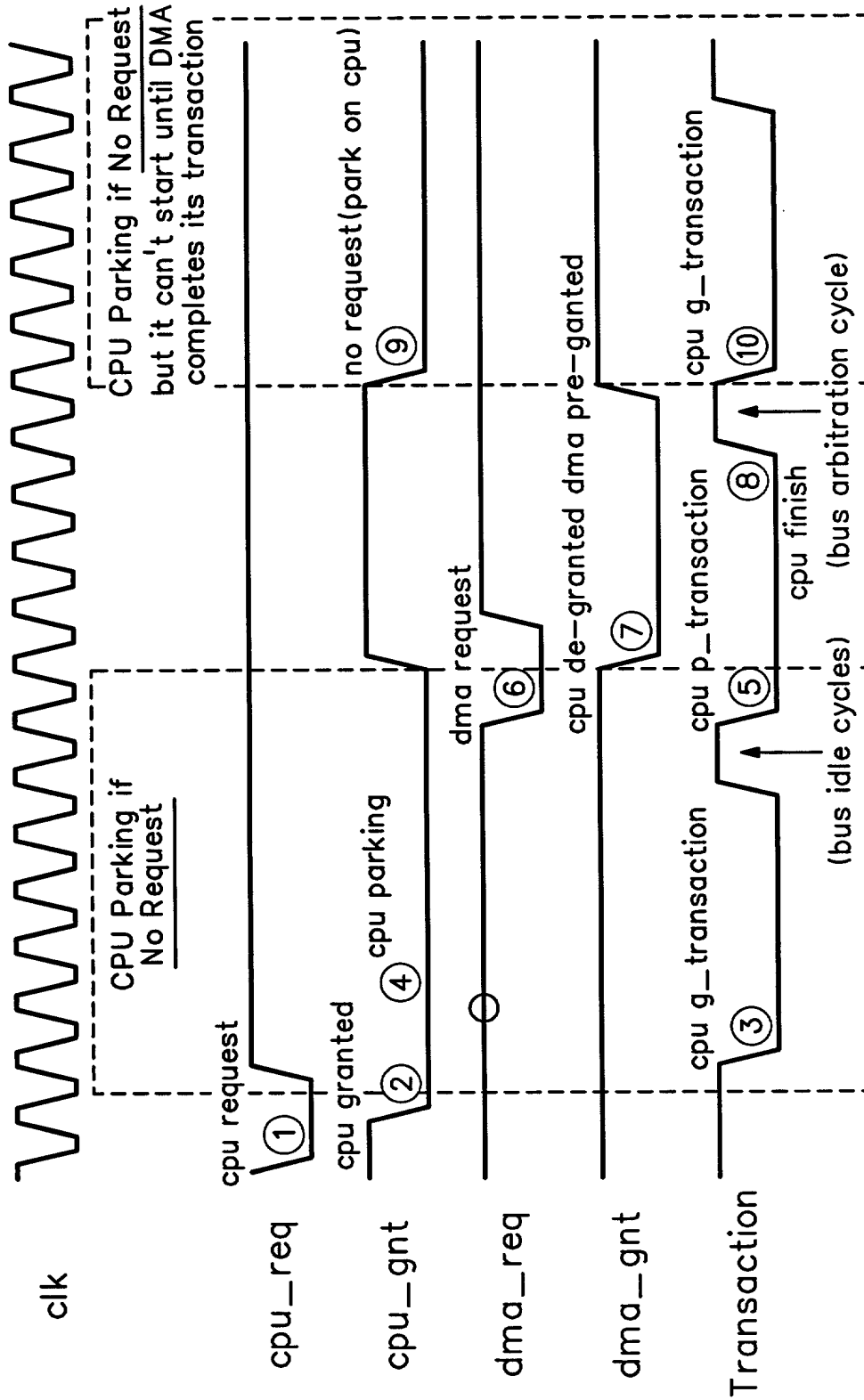


FIG.8
 ARBITRATION PROTOCOL EXAMPLE
 PARKING

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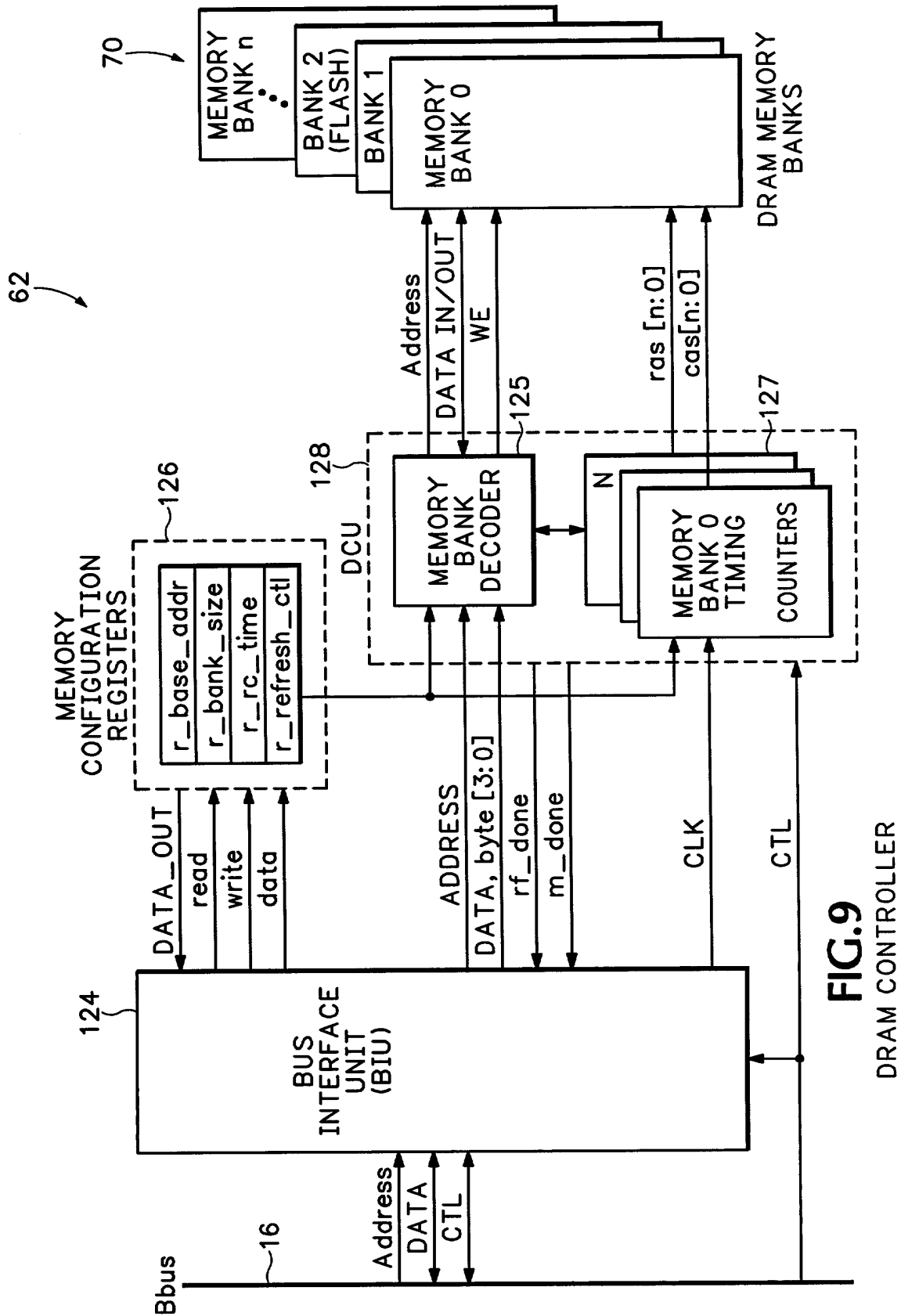
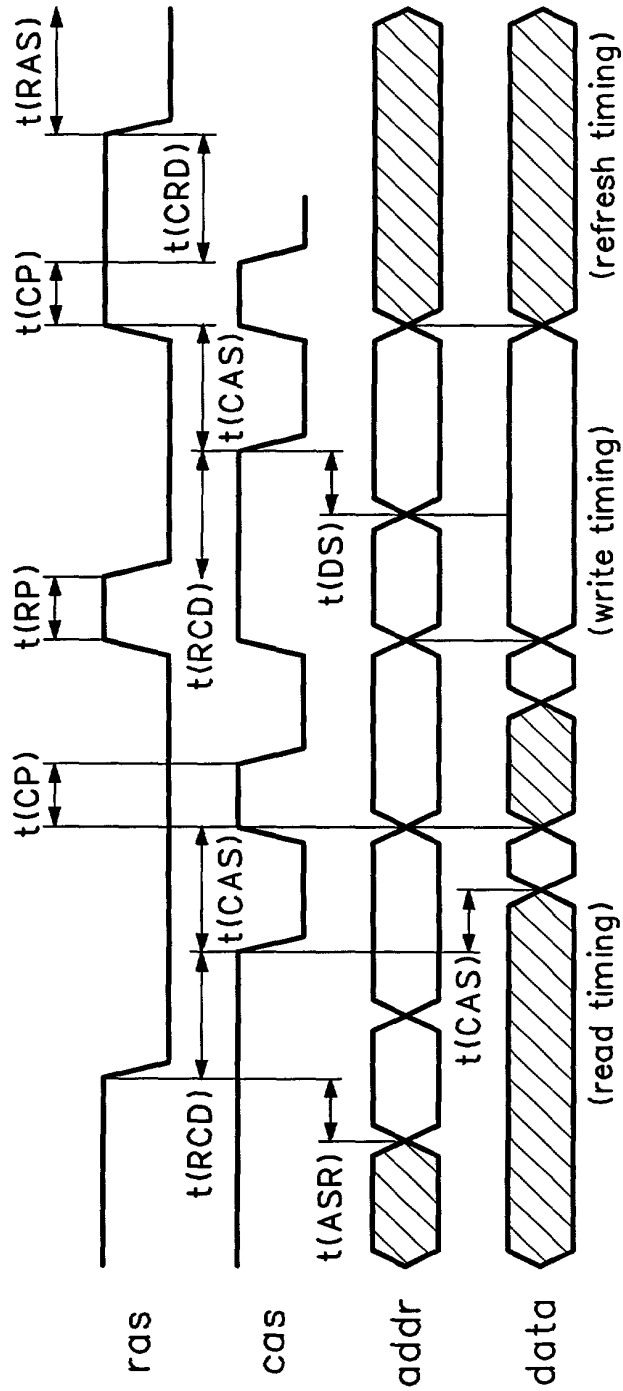
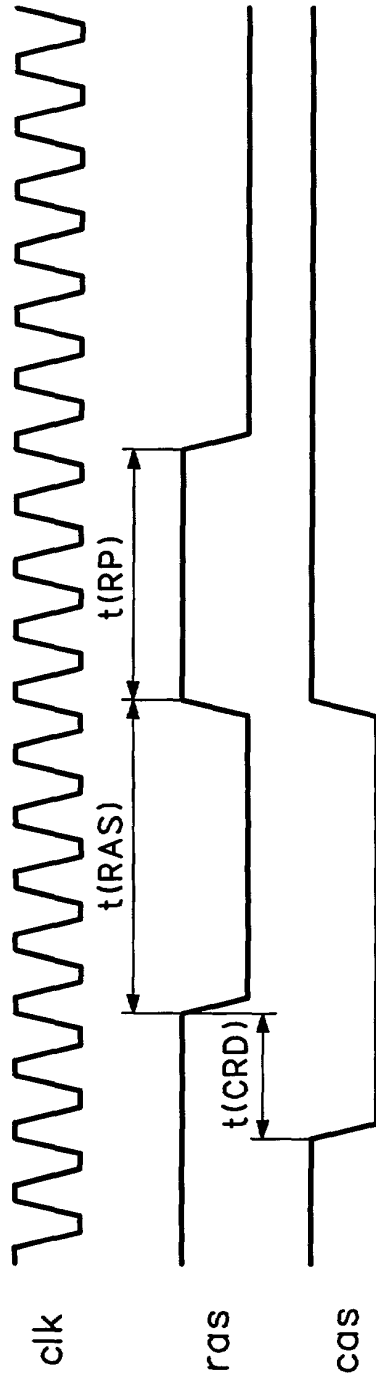


FIG. 9
 DRAM CONTROLLER

DRAM REFRESH CAS BEFORE RAS TIMING



RAS/CAS SERIALIZED TIMING CONSIDERATIONS

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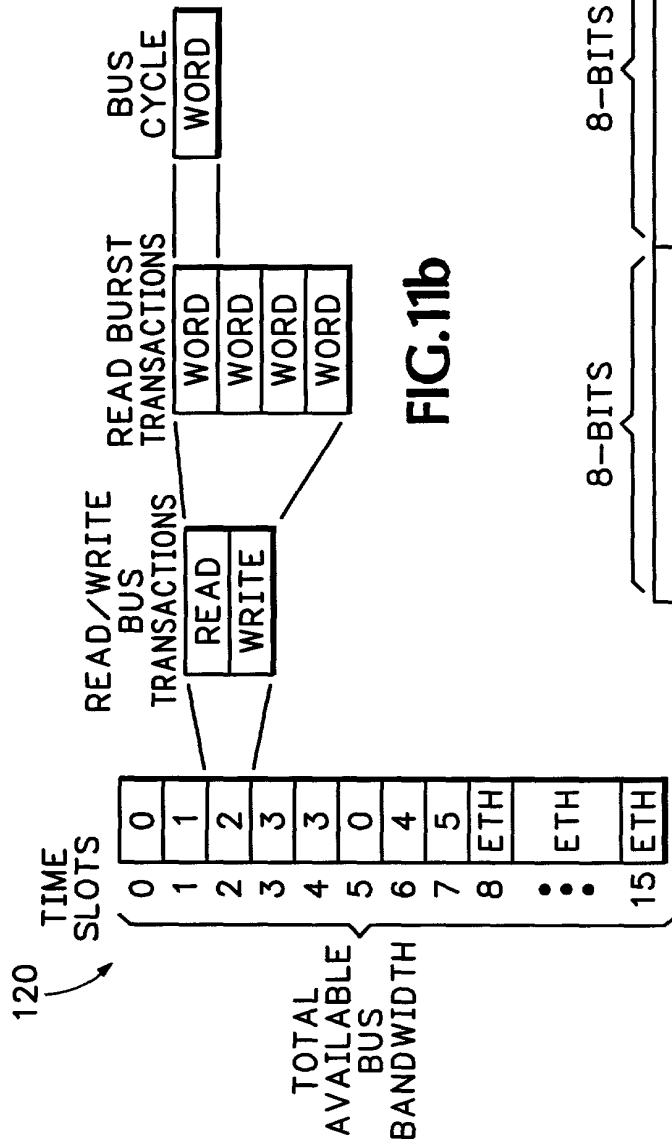


FIG. 11b

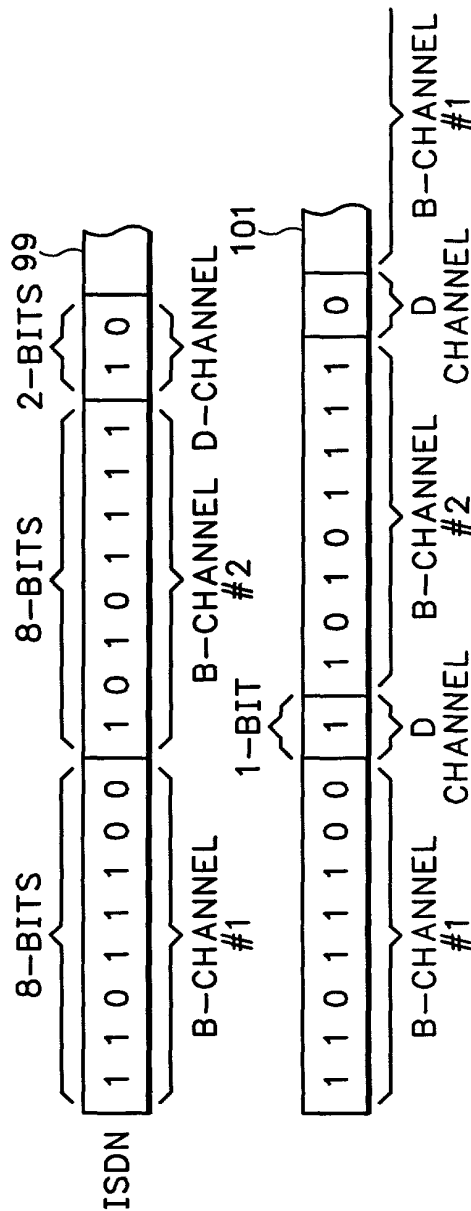


FIG. 12

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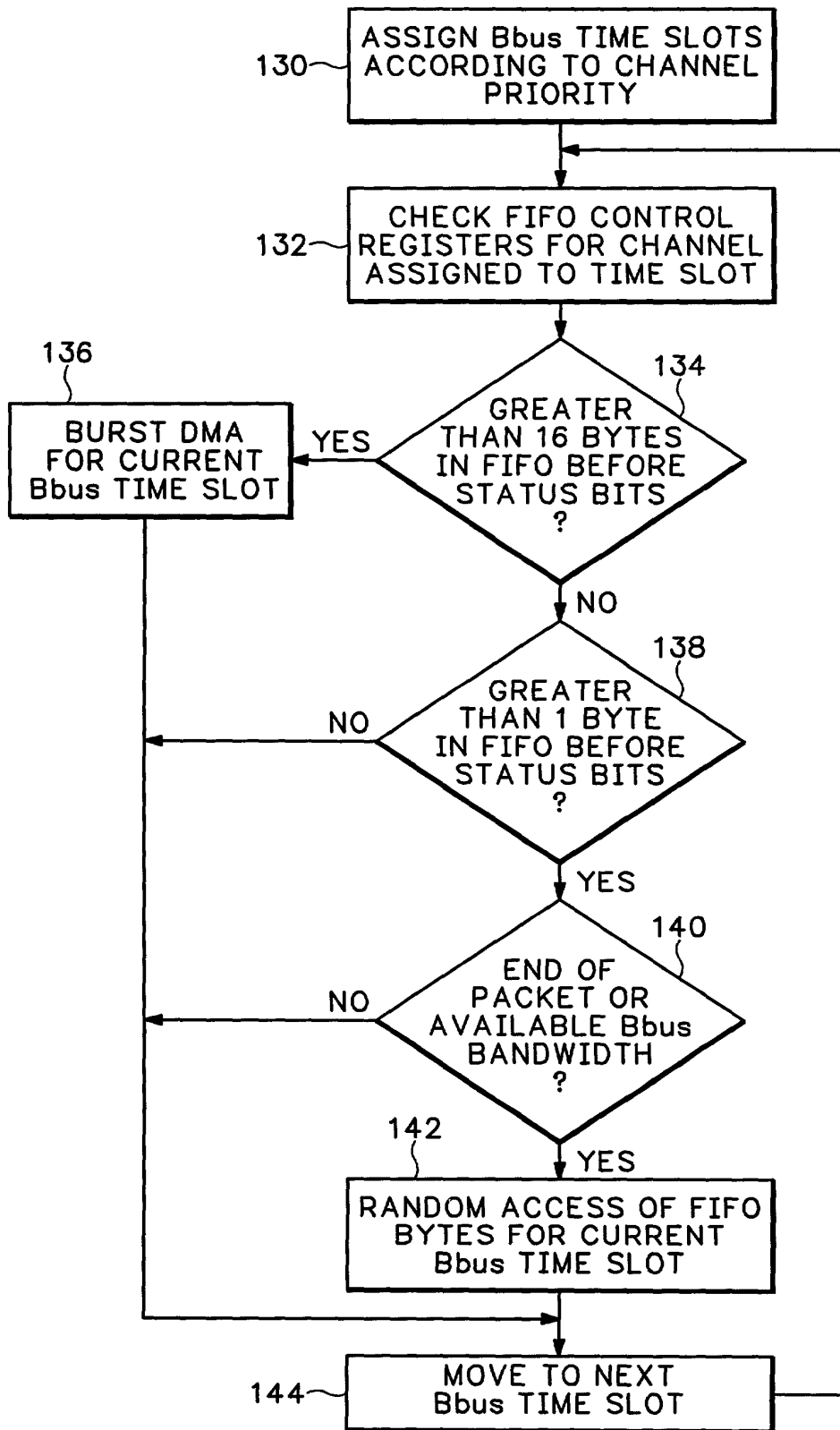


FIG.13

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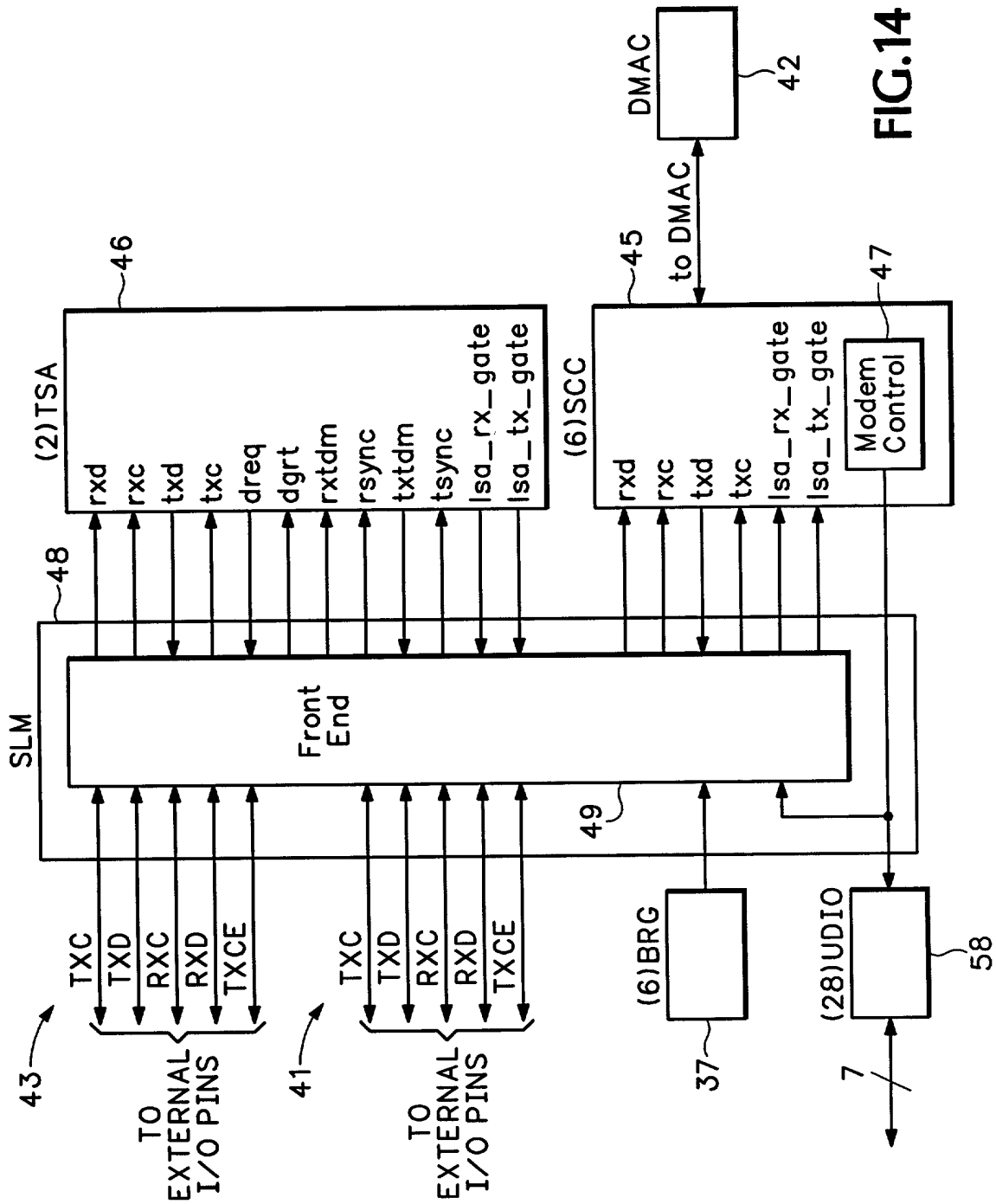


FIG.14



FIG.15

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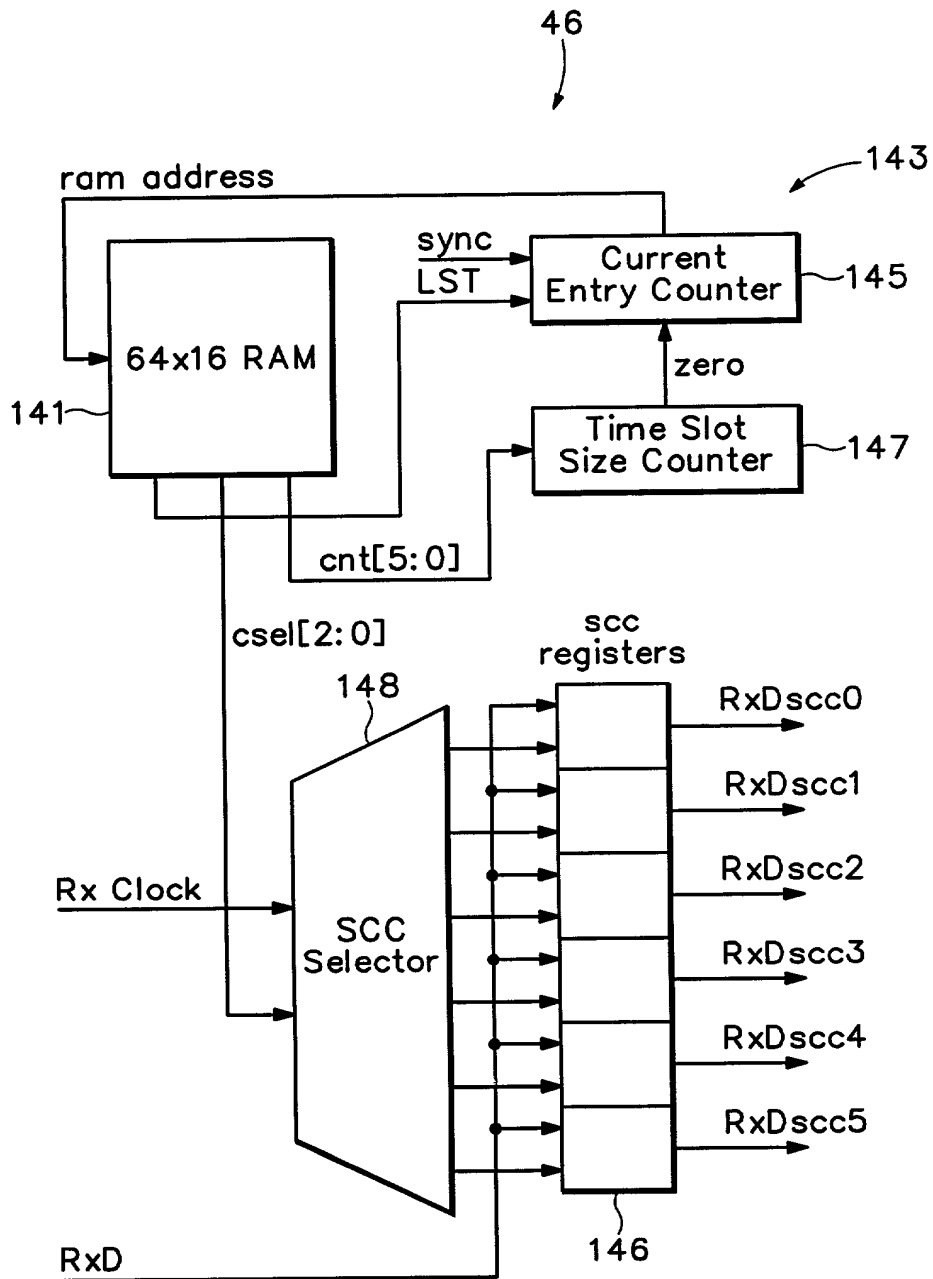


FIG.16
TSA RECEIVE
BLOCK DIAGRAM

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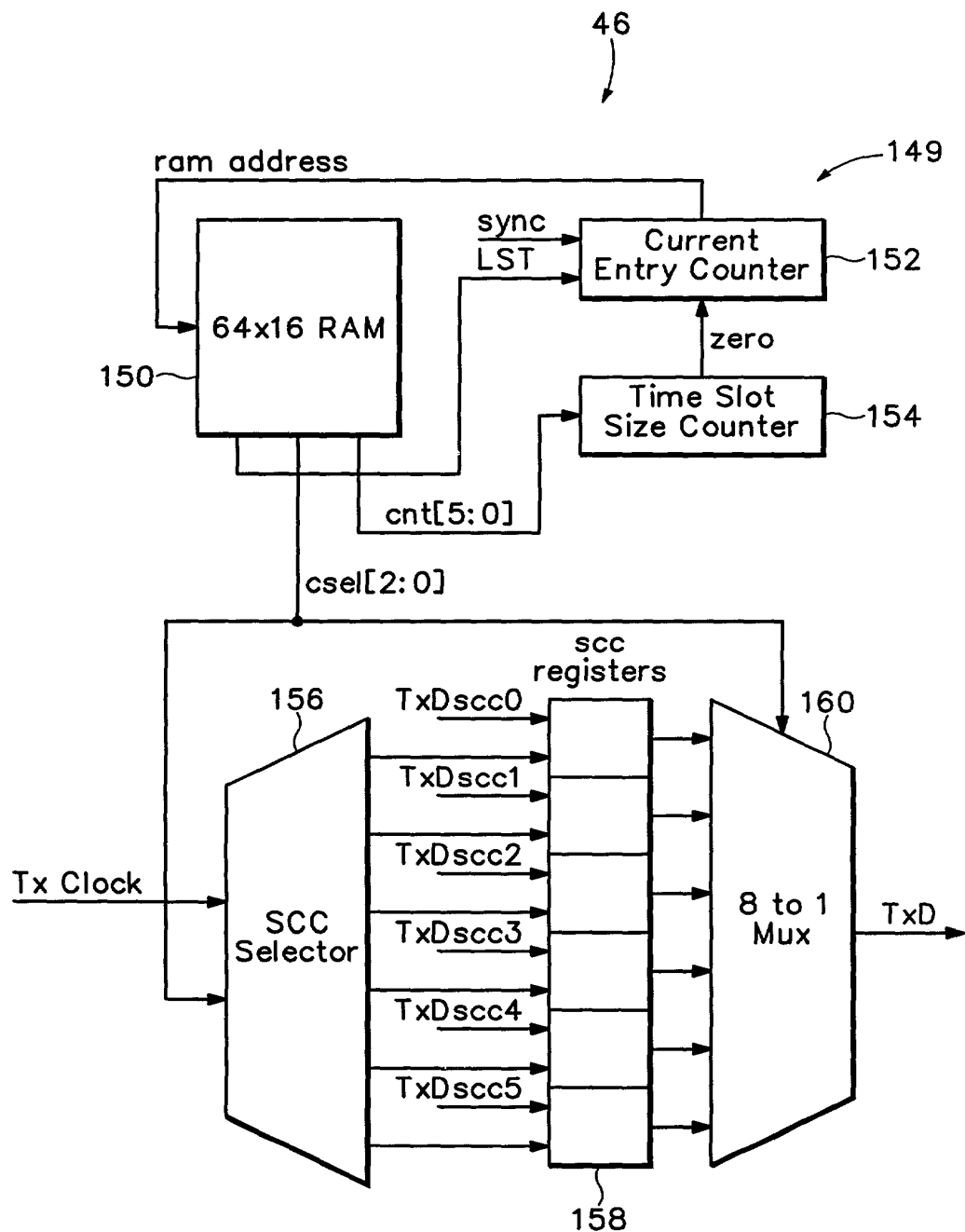


FIG.17
 TSA TRANSMIT
 BLOCK DIAGRAM

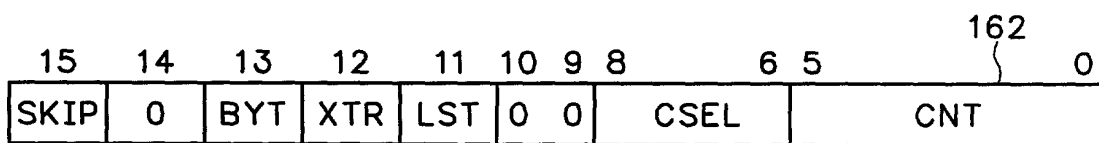


FIG.18

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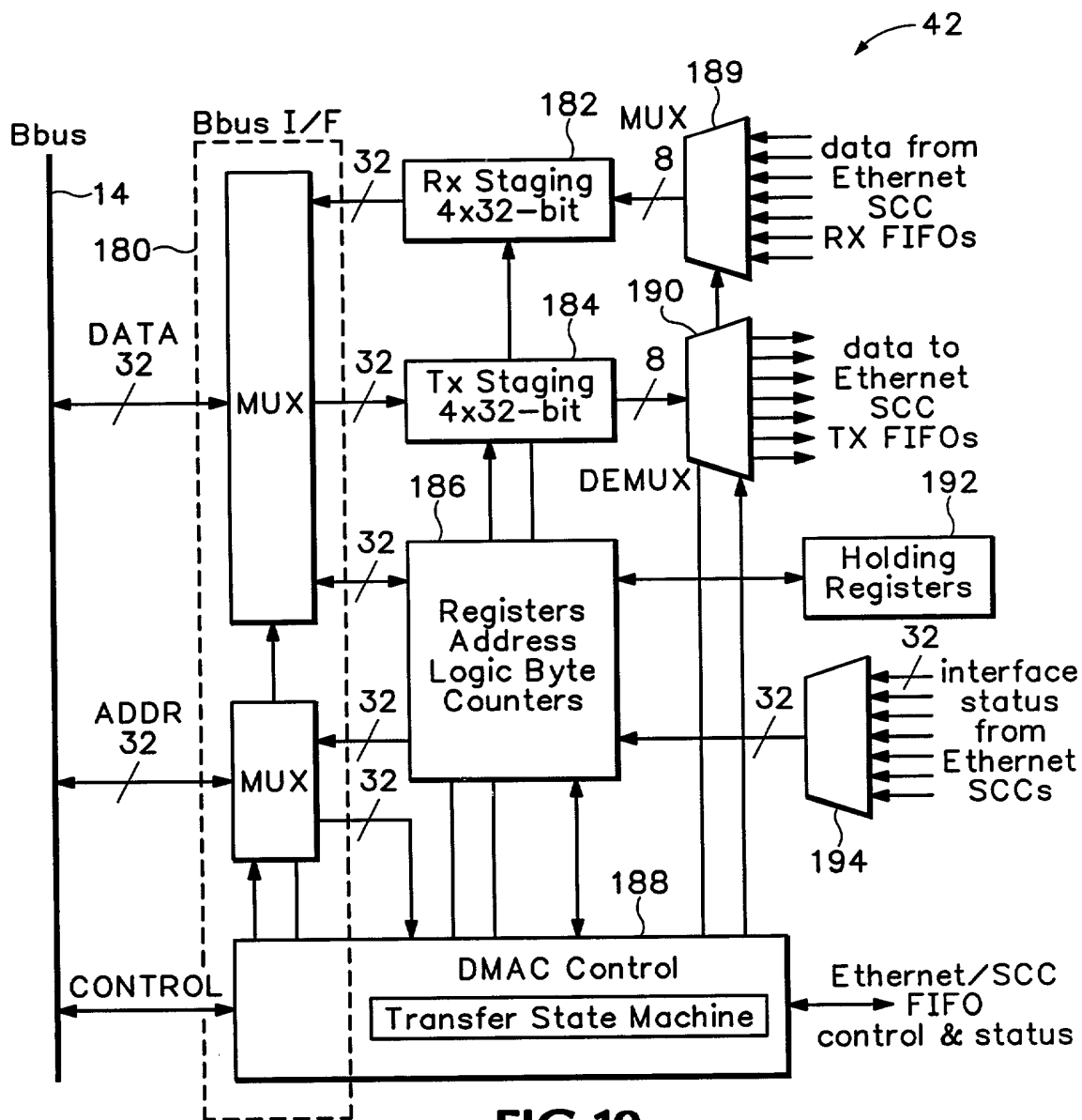


FIG. 19
 DMAC BLOCK DIAGRAM

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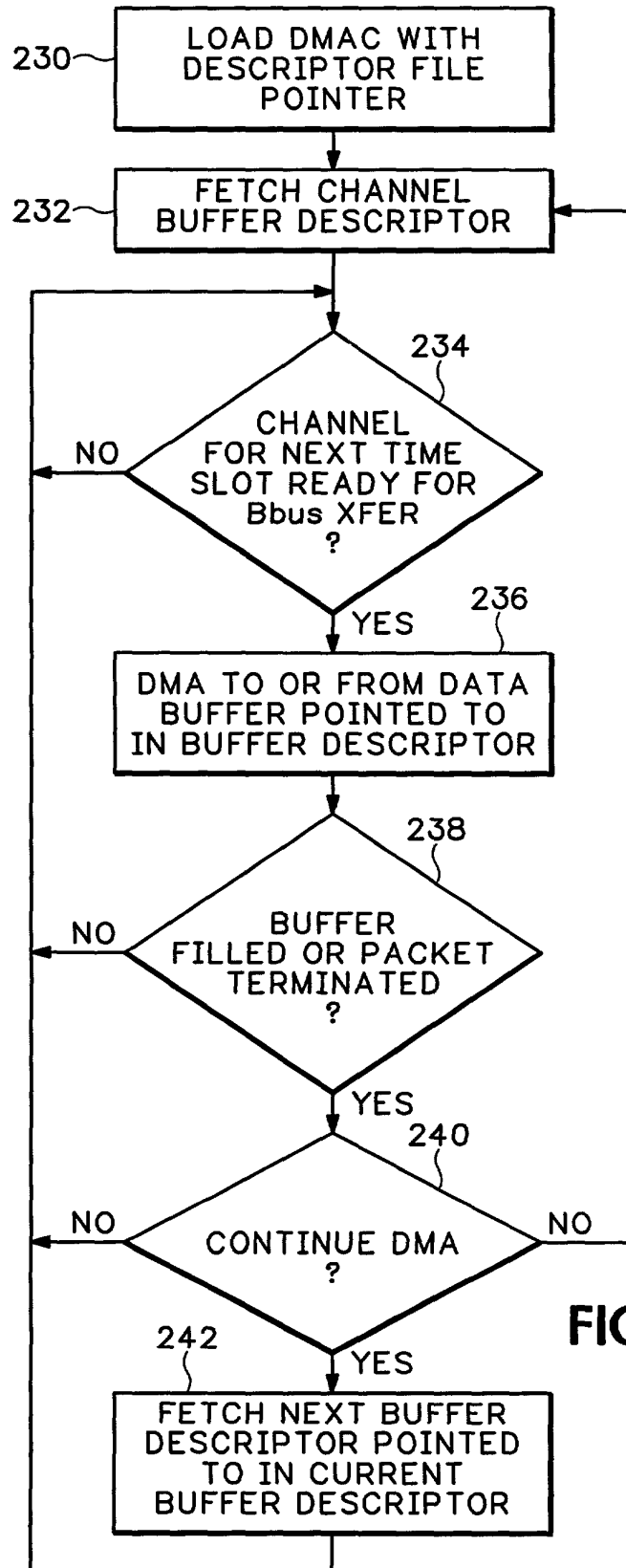


FIG.20

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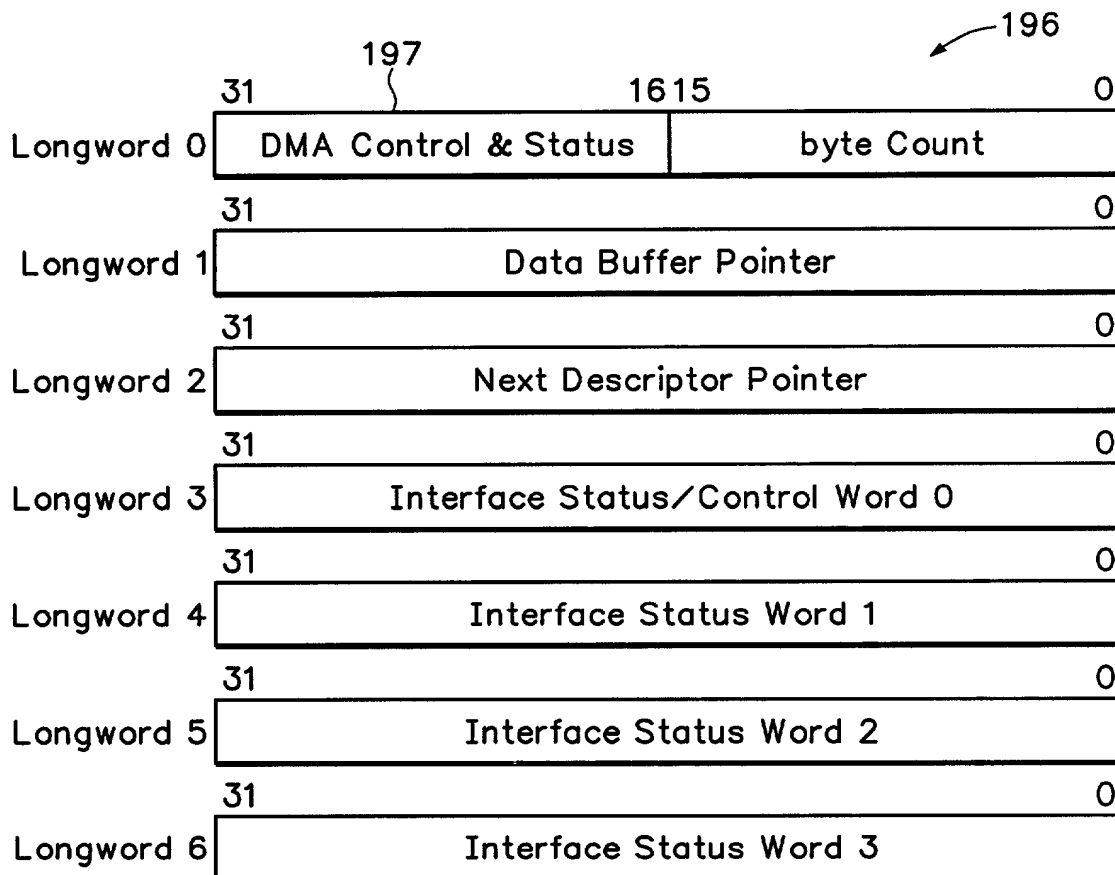


FIG.21
 BUFFER DESCRIPTOR

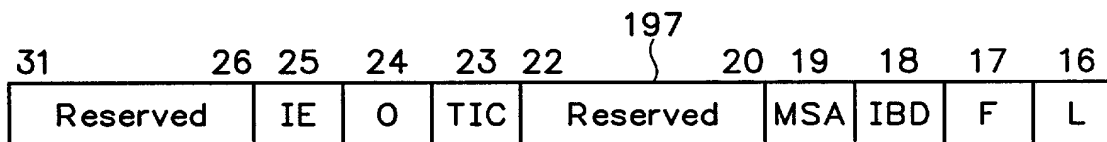


FIG.22
 DMA CONTROL & STATUS
 FIELD OF DESCRIPTOR

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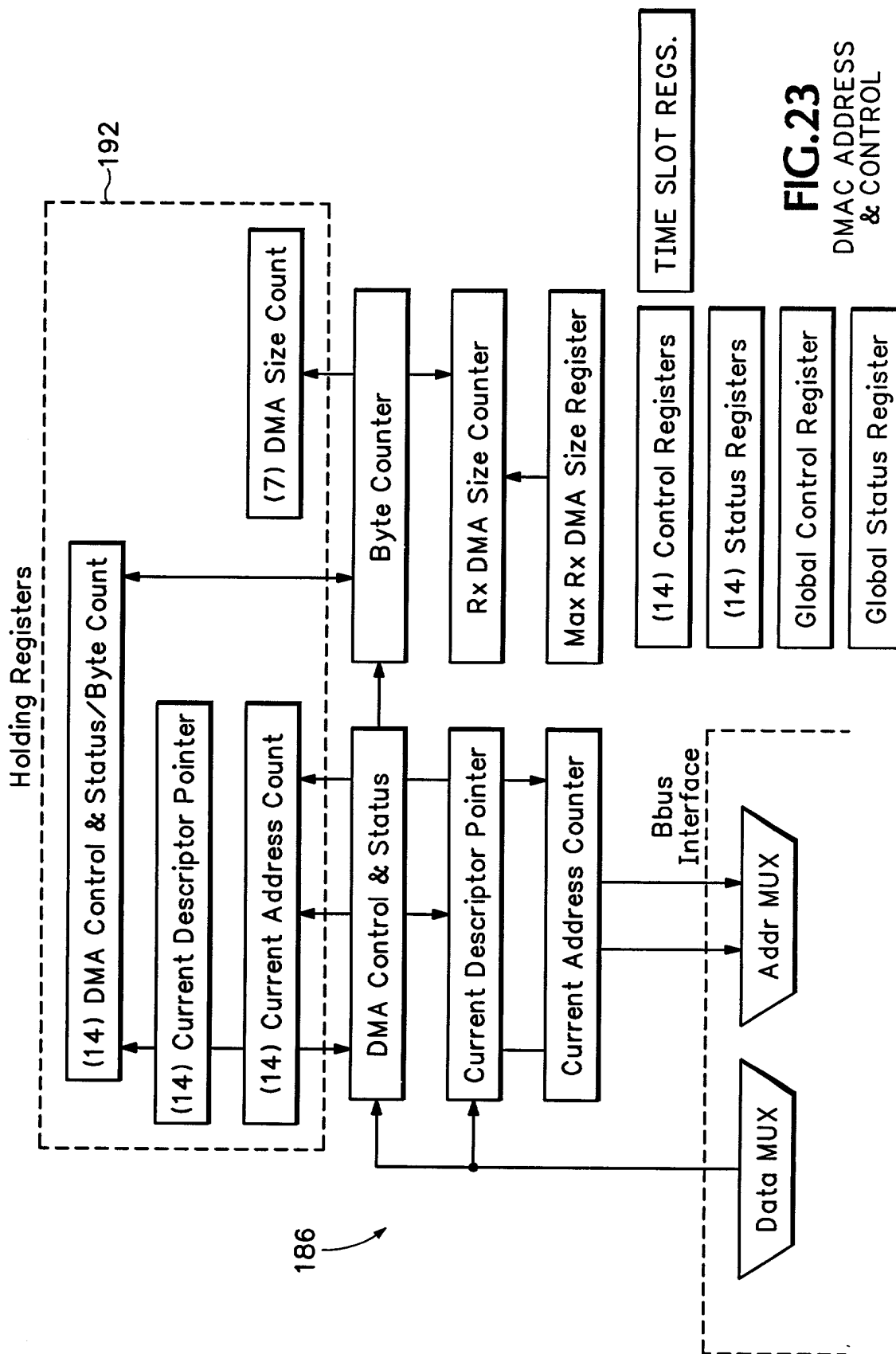


FIG. 23
 DMAC ADDRESS
 & CONTROL

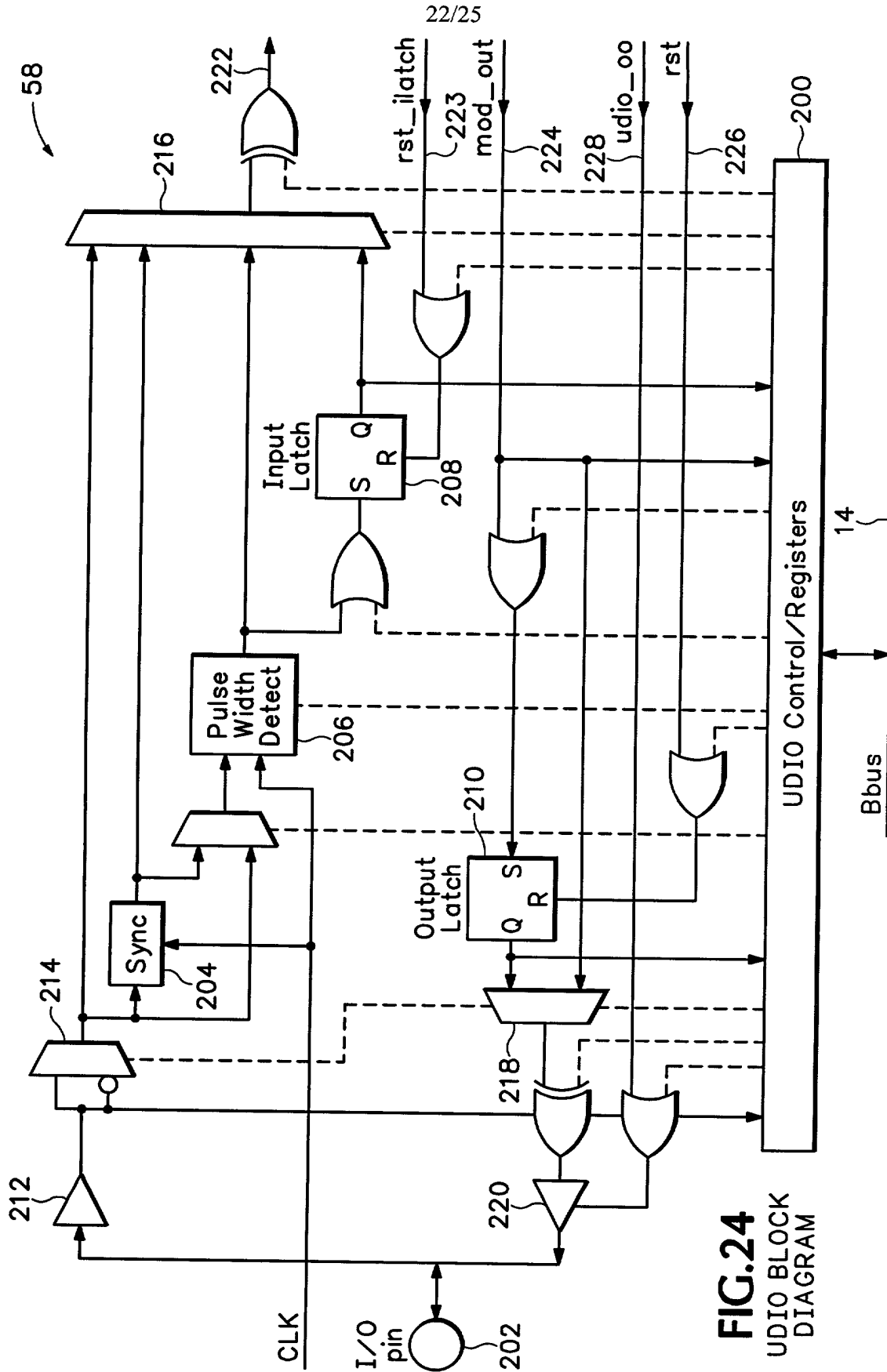


FIG. 24
 UDIO BLOCK
 DIAGRAM

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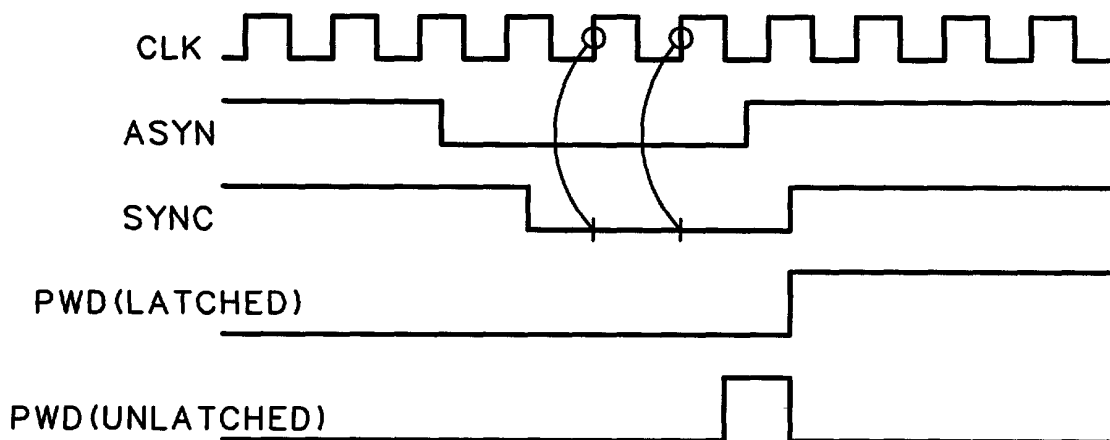


FIG.25

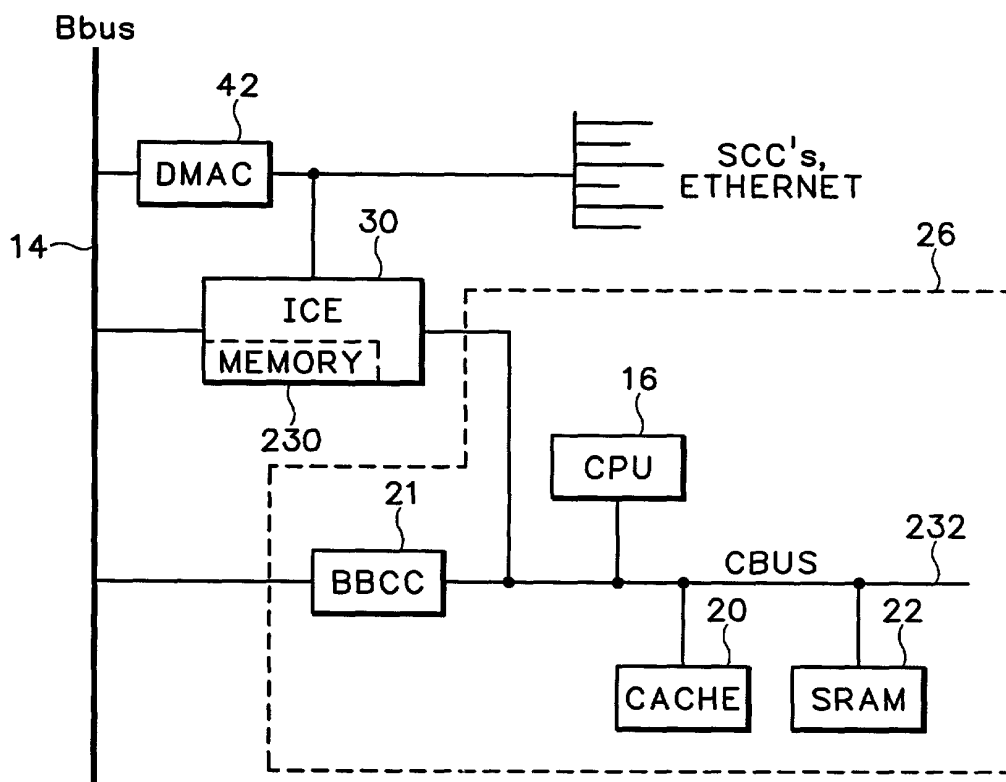
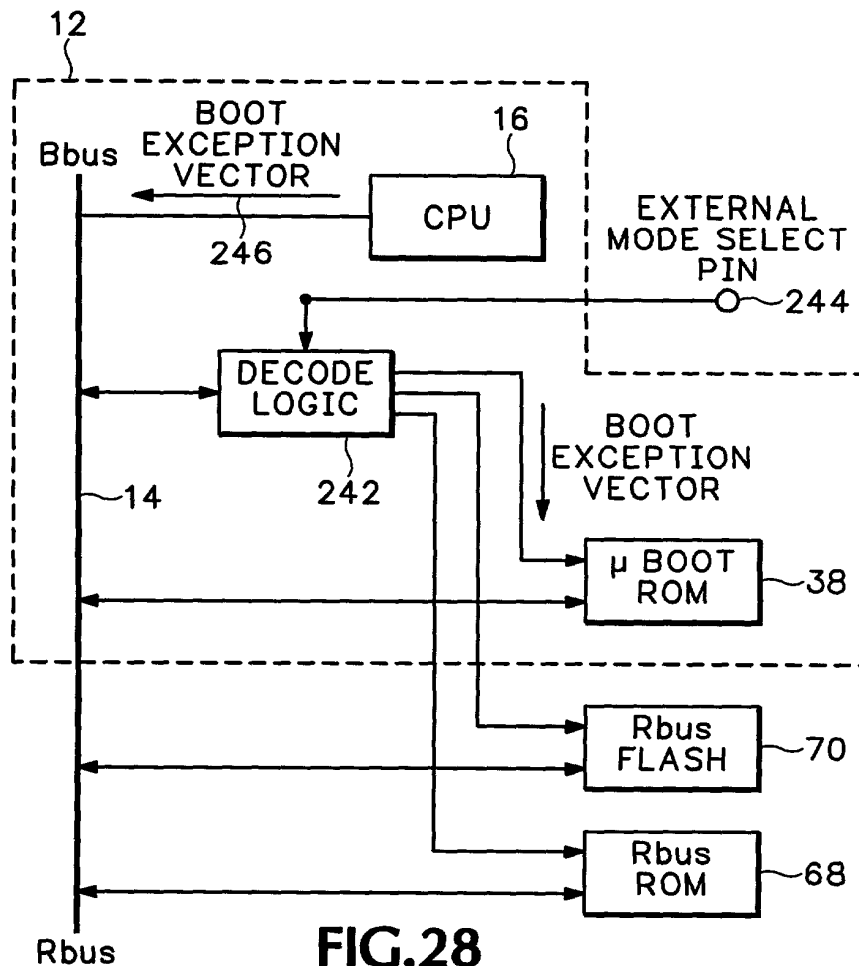
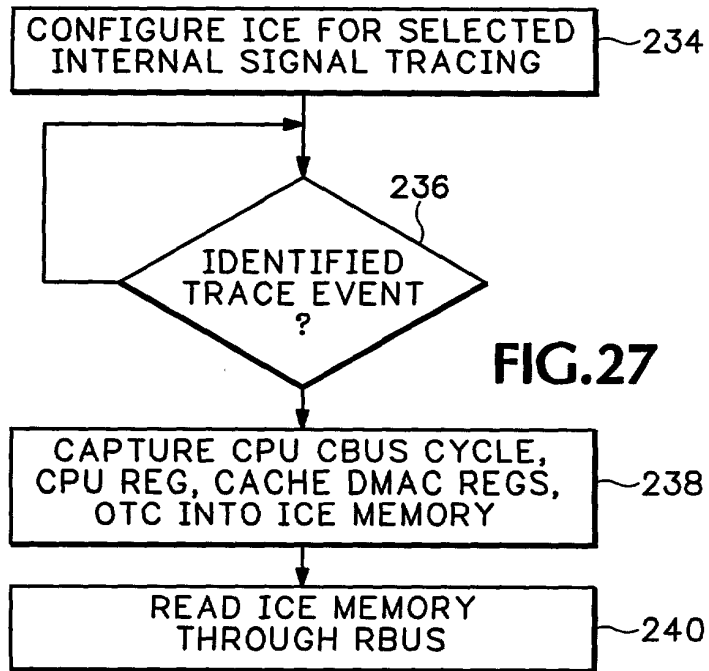


FIG.26

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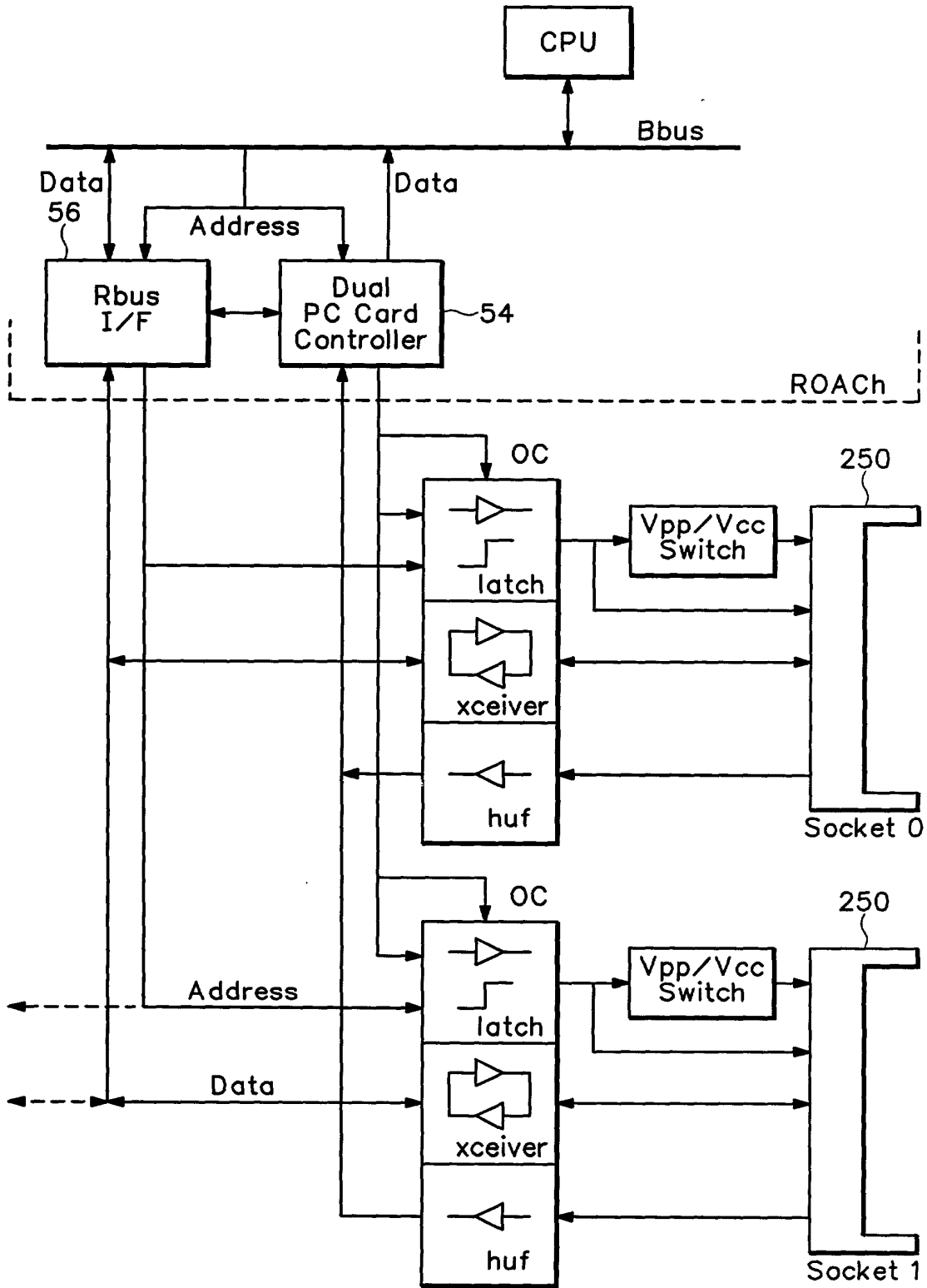


FIG.29
PC CARD INTERFACE